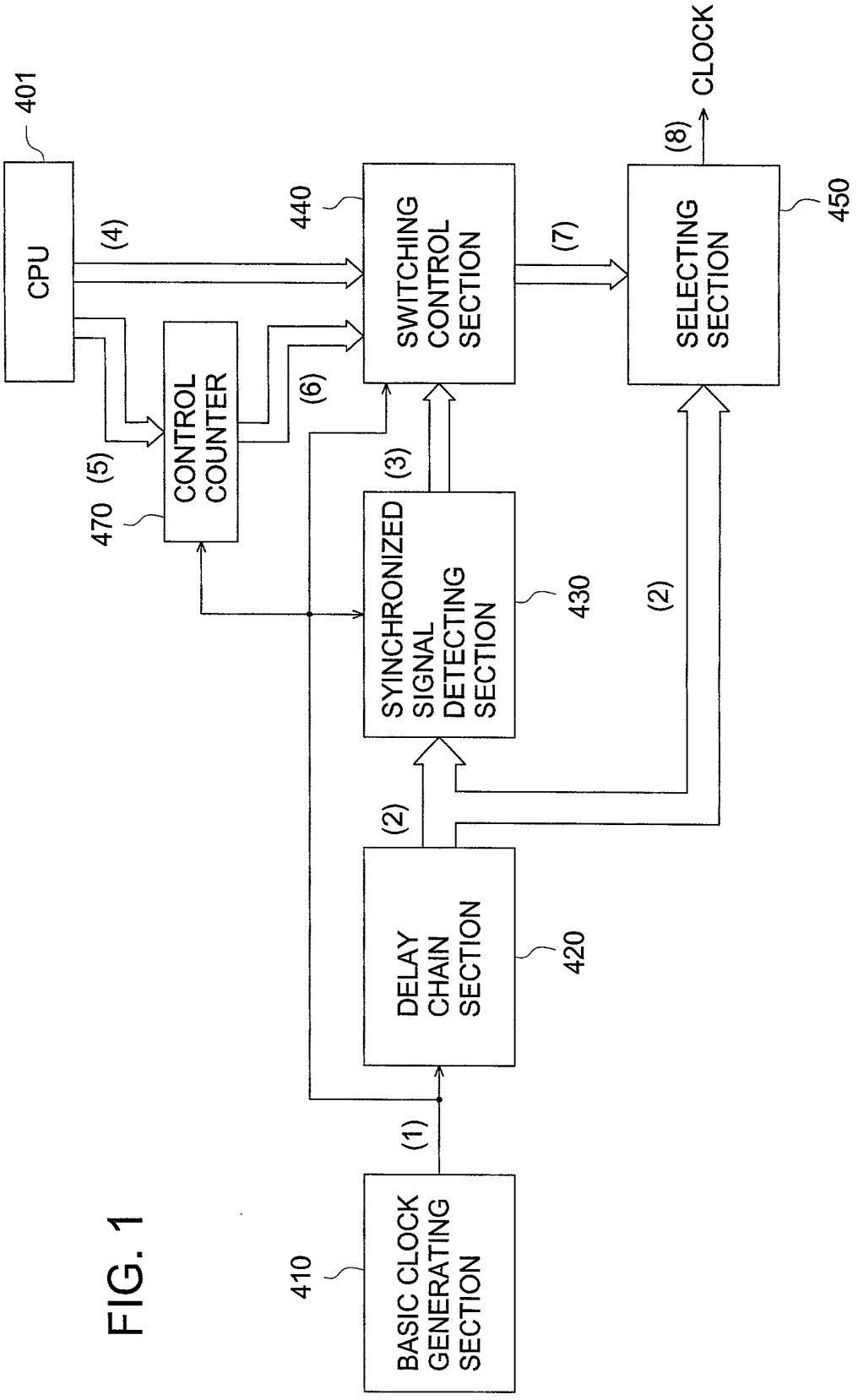

401
CPU
(4)
440
SWITCHING CONTROL SECTION
(7)
(8)
CLOCK
450
SELECTING SECTION
CONTROL COUNTER
(6)
(5)
470
(3)
SYINCHRONIZED SIGNAL DETECTING SECTION
430
(2)
(2)
DELAY CHAIN SECTION
420
(1)
410
BASIC CLOCK GENERATING SECTION

FIG. 1

FIG. 2 (a)

BASIC CLOCK

FIG. 2 (b)

DL19

FIG. 2 (c)

DL20

FIG. 2 (d)

DL21

FIG. 2 (e)

DL22

FIG. 2 (f)

DL23

FIG. 2 (g)

DL24

FIG. 2 (h)

DL25

FIG. 2 (i)

DL46

FIG. 2 (j)

DL47

FIG. 2 (k)

DL48

FIG. 2 (l)

DL49

FIG. 2 (m)

DL50

FIG. 2 (n)

DL51

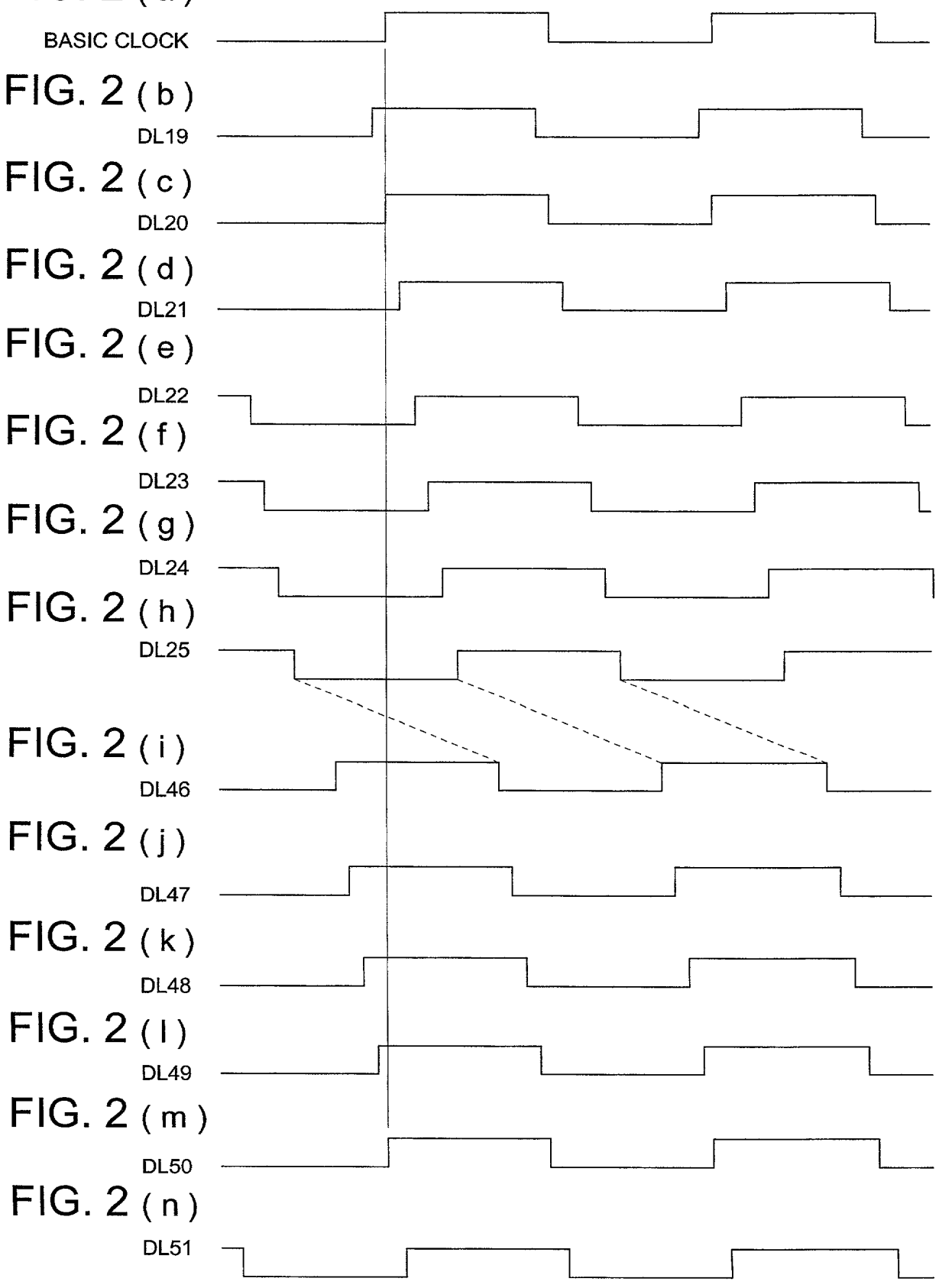


FIG. 3

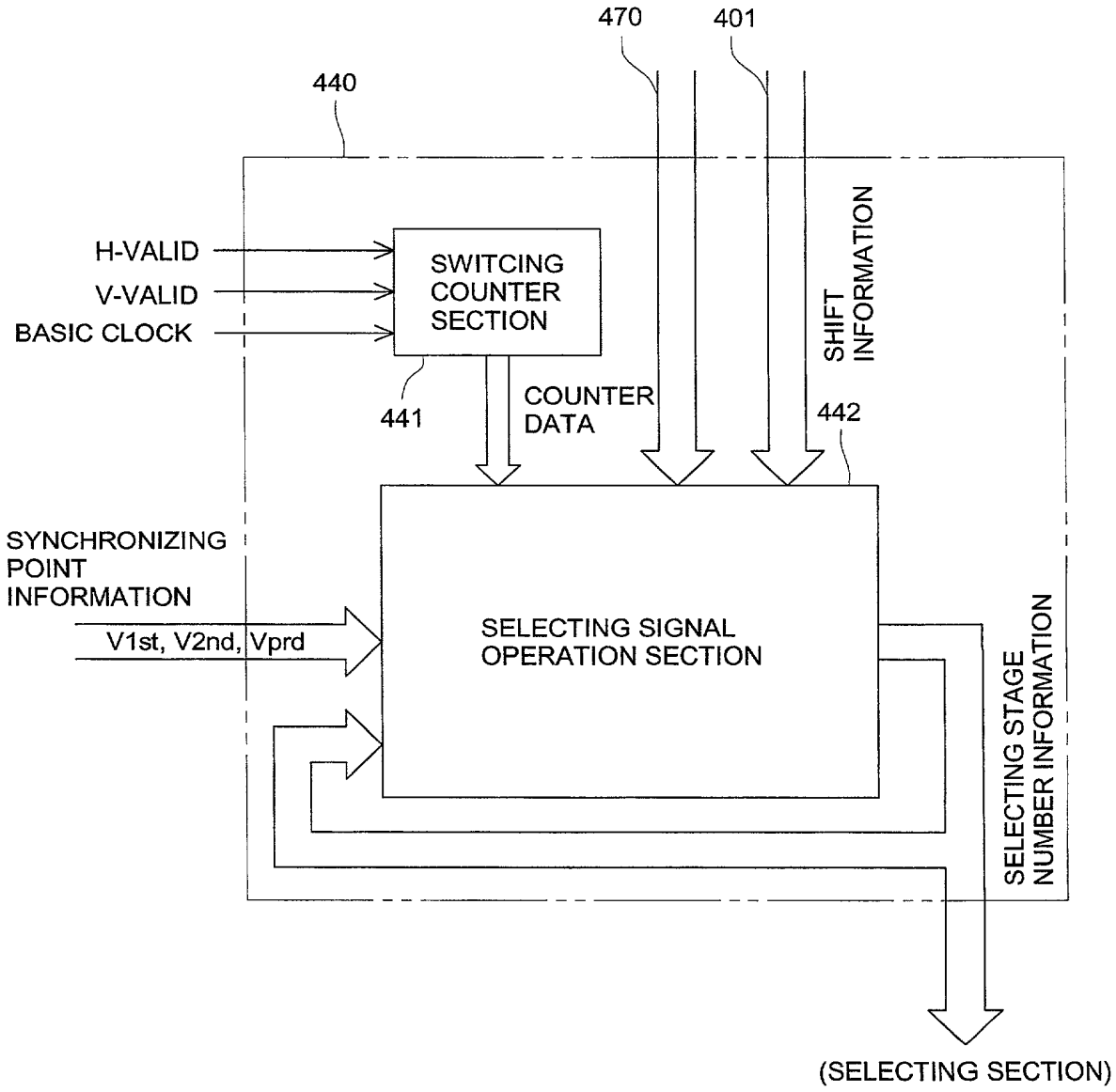

470
401
440
H-VALID
V-VALID
BASIC CLOCK
SWITCING COUNTER SECTION
SHIFT INFORMATION
441
COUNTER DATA
442
SYNCHRONIZING POINT INFORMATION
V1st, V2nd, Vprd
SELECTING SIGNAL OPERATION SECTION
SELECTING STAGE NUMBER INFORMATION
(SELECTING SECTION)

FIG. 4 (a)

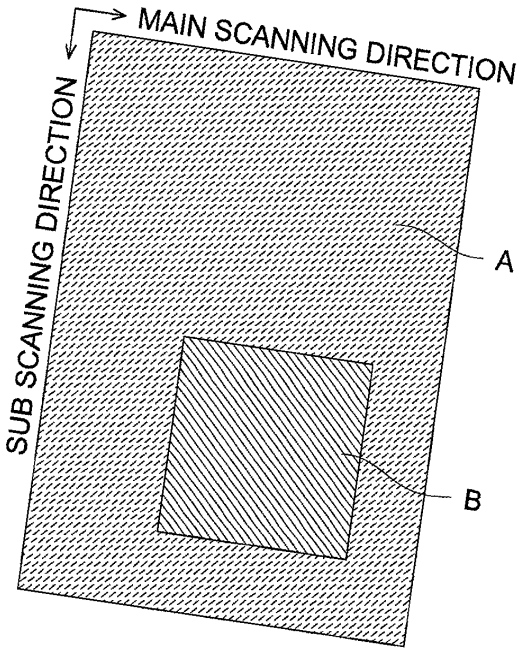
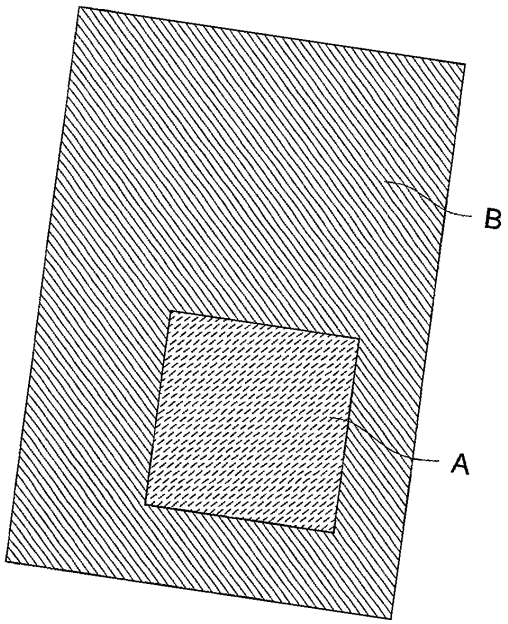


FIG. 4 (b)



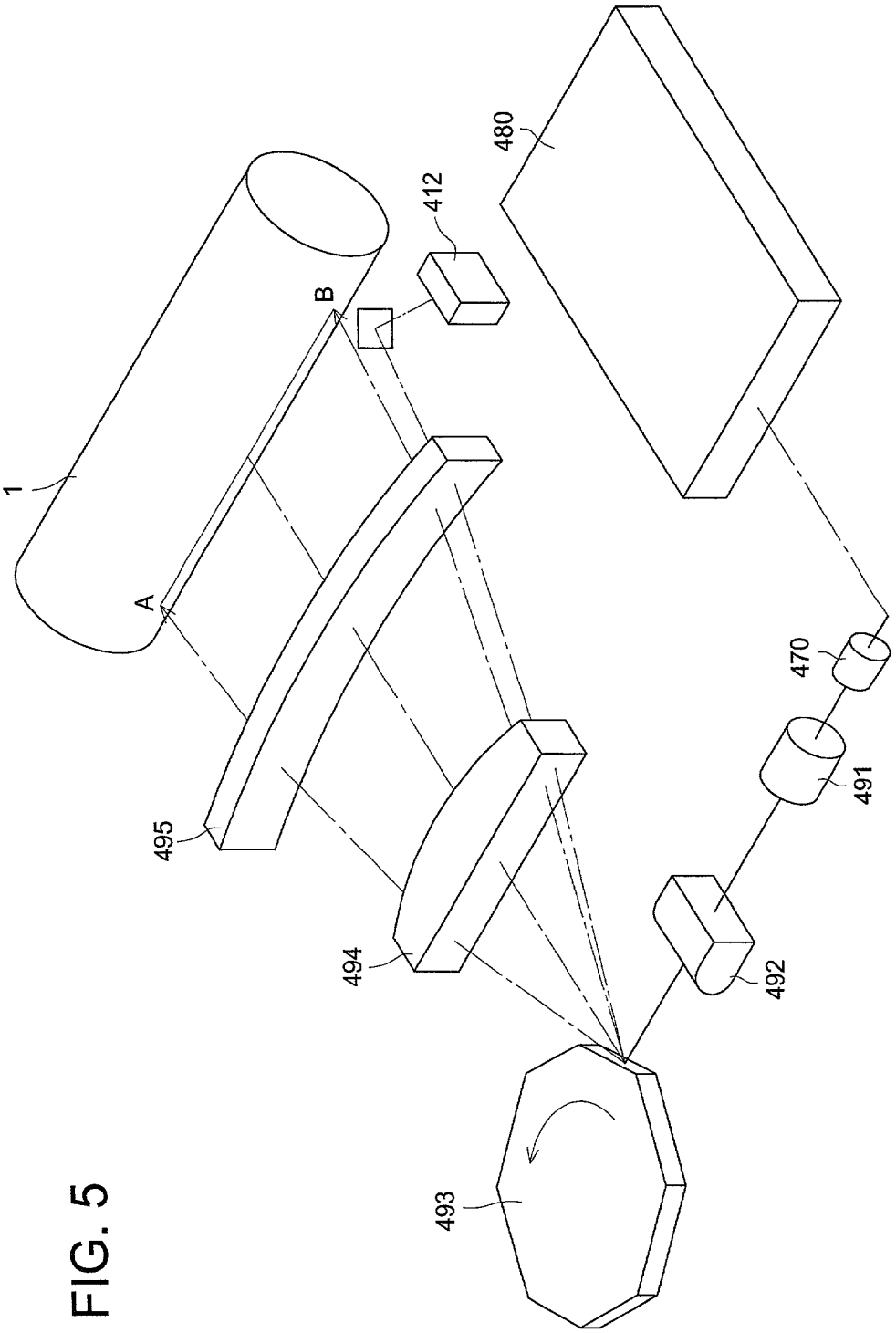


FIG. 5

FIG. 6

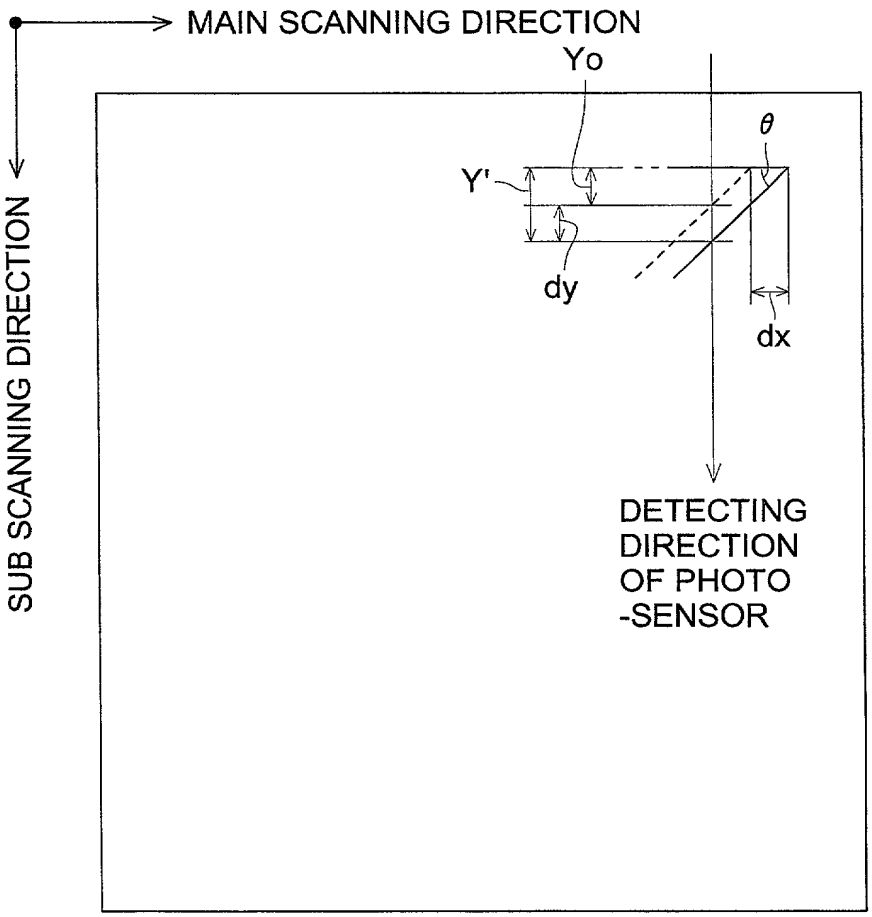

MAIN SCANNING DIRECTION
SUB SCANNING DIRECTION
Yo
θ
Y'
dy
dx
DETECTING
DIRECTION
OF PHOTO
-SENSOR

FIG. 7 (a)

FIG. 7 (b)

FIG. 7 (c)

FIG. 7 (d)

FIG. 7 (e)

FIG. 7 (f)

FIG. 7 (g)

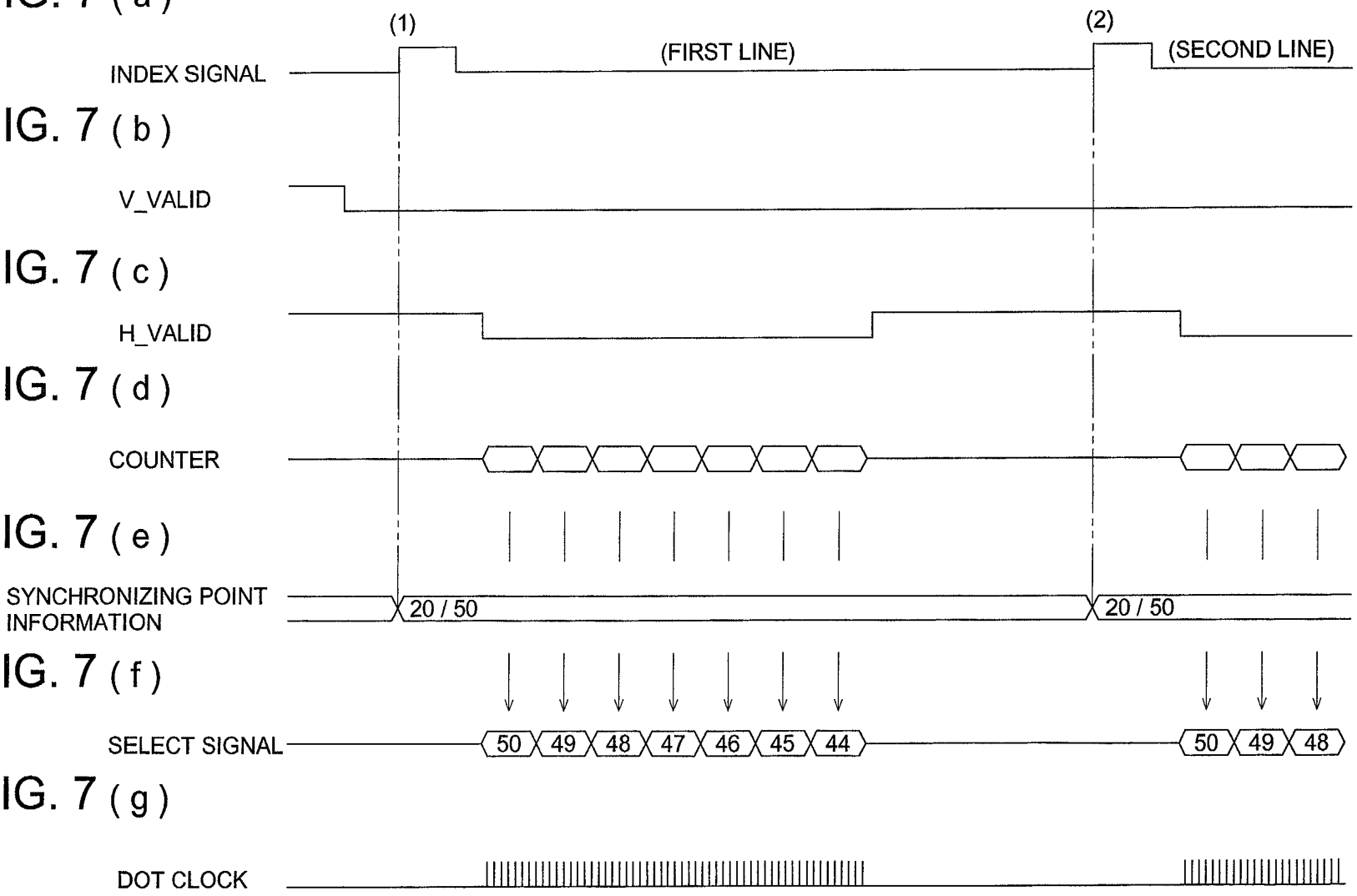


FIG. 8 (a)

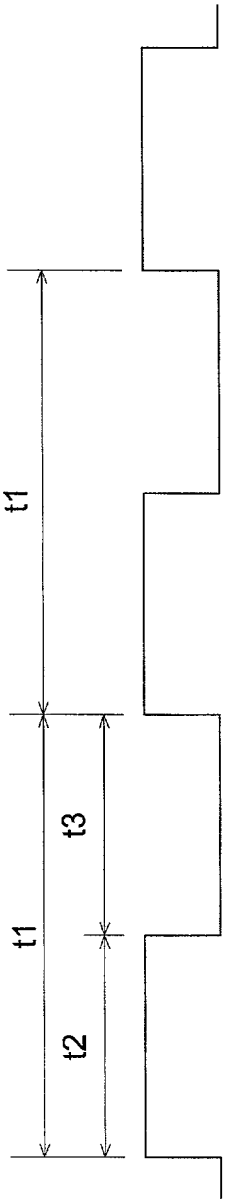
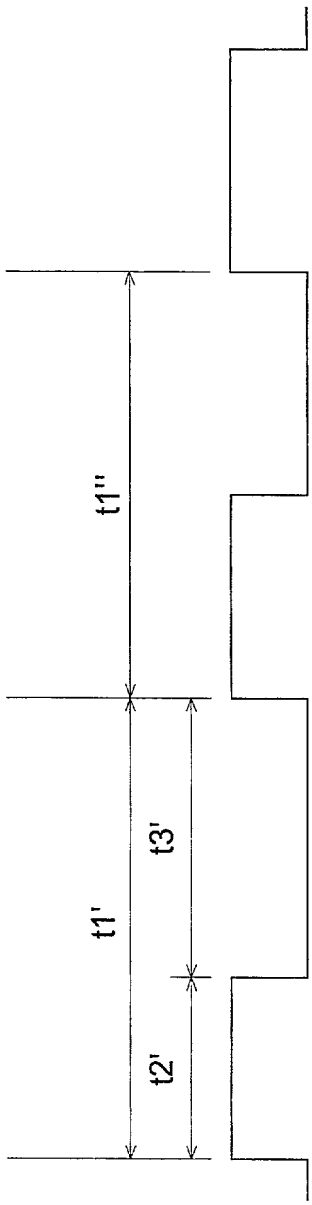


FIG. 8 (b)



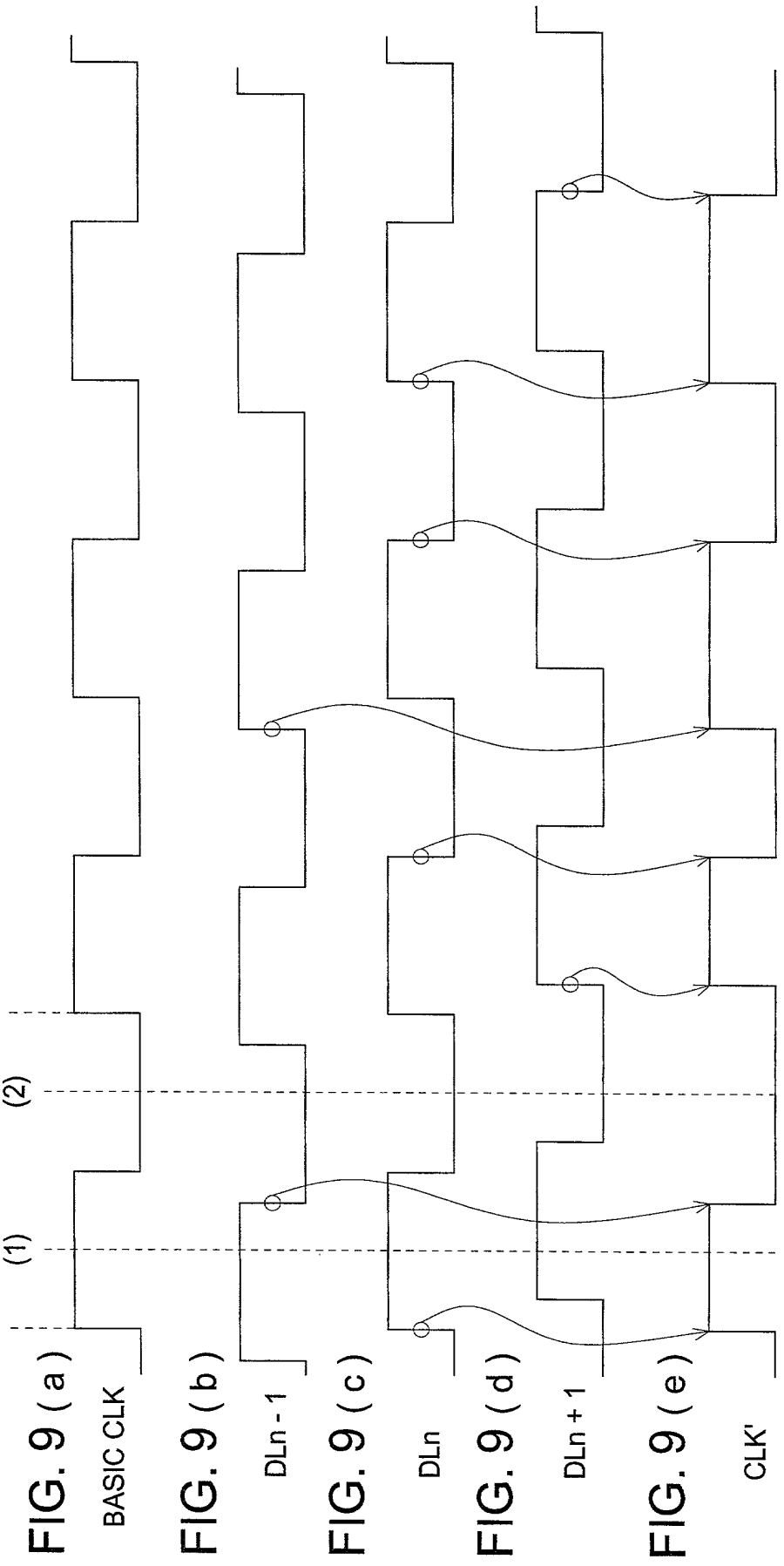


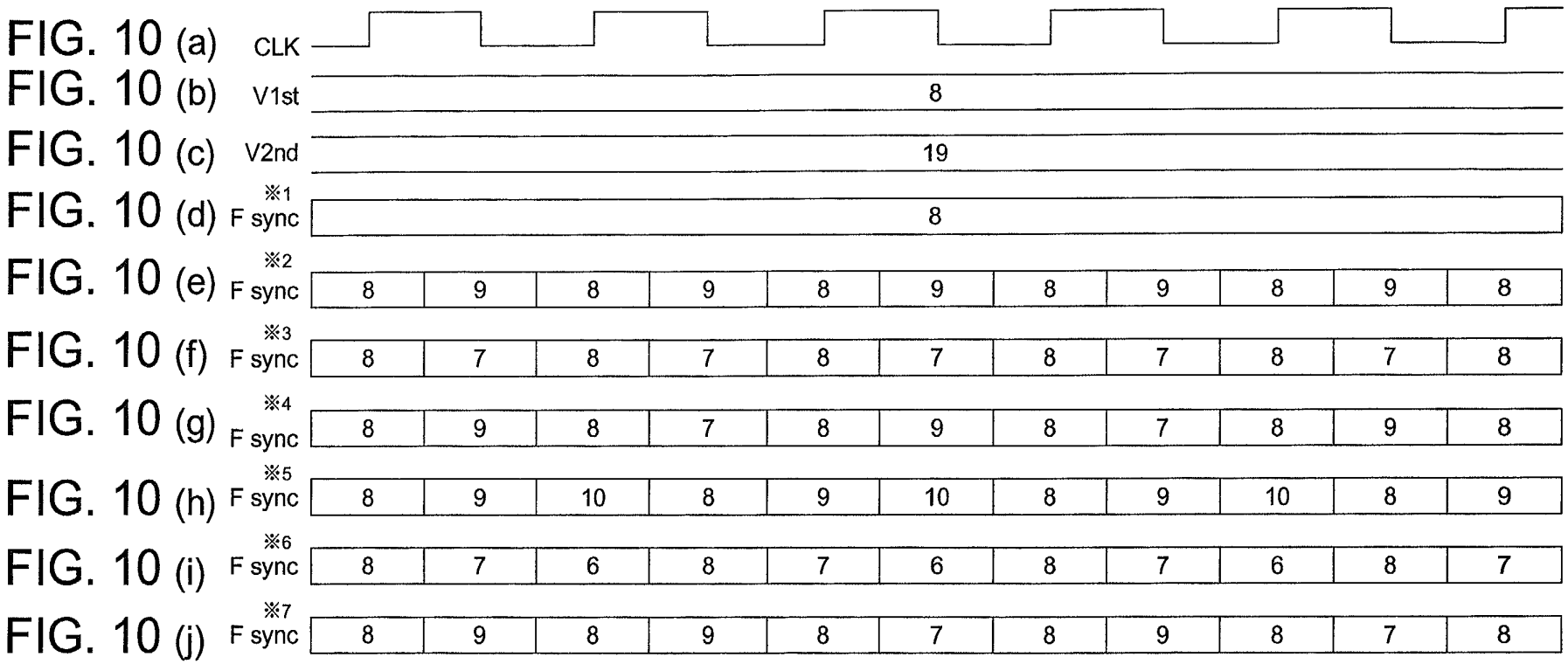
FIG. 9 (a)

FIG. 9 (b)

FIG. 9 (c)

FIG. 9 (d)

FIG. 9 (e)



※1	Fsync IN THE CASE WHERE NO SIGNAL CONTROL IS DONE	[REVICEdata=0]
※2	Fsync IN THE CASE WHERE SIGNAL CONTROL IS ONCE DONE IN ＋ DIRECTION	[REVICEdata=1, TIMESdata=1, MODEdata=00]
※3	Fsync IN THE CASE WHERE SIGNAL CONTROL IS ONCE DONE IN － DIRECTION	[REVICEdata=1, TIMESdata=1, MODEdata=11]
※4	Fsync IN THE CASE WHERE SIGNAL CONTROL IS ONCE DONE IN ± DIRECTION	[REVICEdata=1, TIMESdata=1, MODEdata=01]
※5	Fsync IN THE CASE WHERE SIGNAL CONTROL IS TWICE DONE IN ＋ DIRECTION	[REVICEdata=1, TIMESdata=2, MODEdata=00]
※6	Fsync IN THE CASE WHERE SIGNAL CONTROL IS TWICE DONE IN － DIRECTION	[REVICEdata=1, TIMESdata=2, MODEdata=11]
※7	Fsync IN THE CASE WHERE SIGNAL CONTROL IS ONCE DONE AT RANDOM	[REVICEdata=1, TIMESdata=1, MODEdata=10]

FIG. 11 (a)

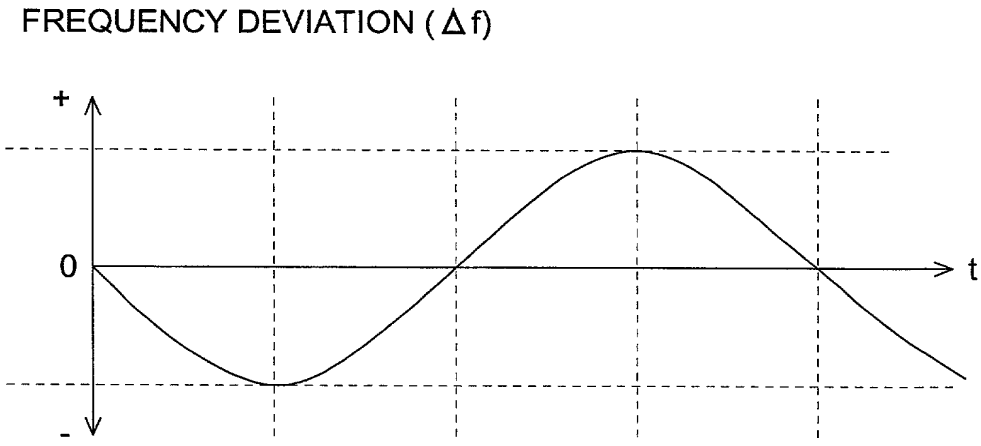


FIG. 11 (b)

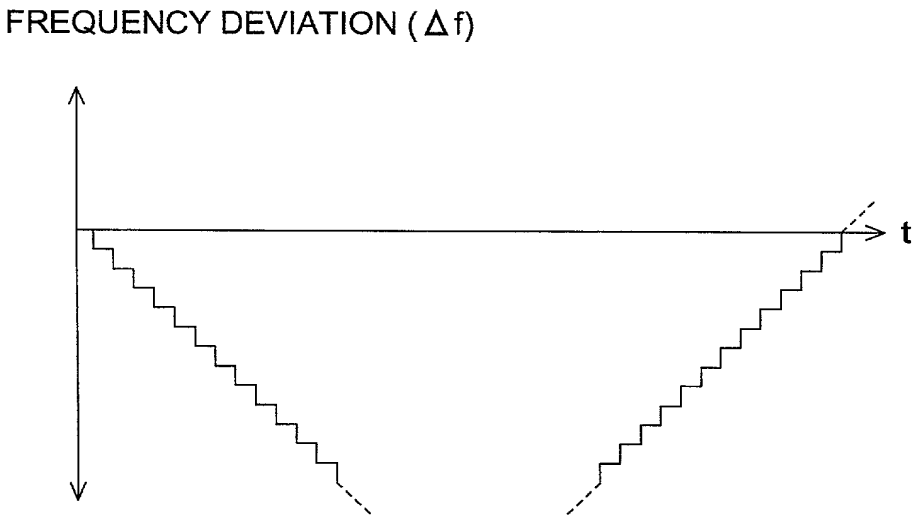


FIG. 12

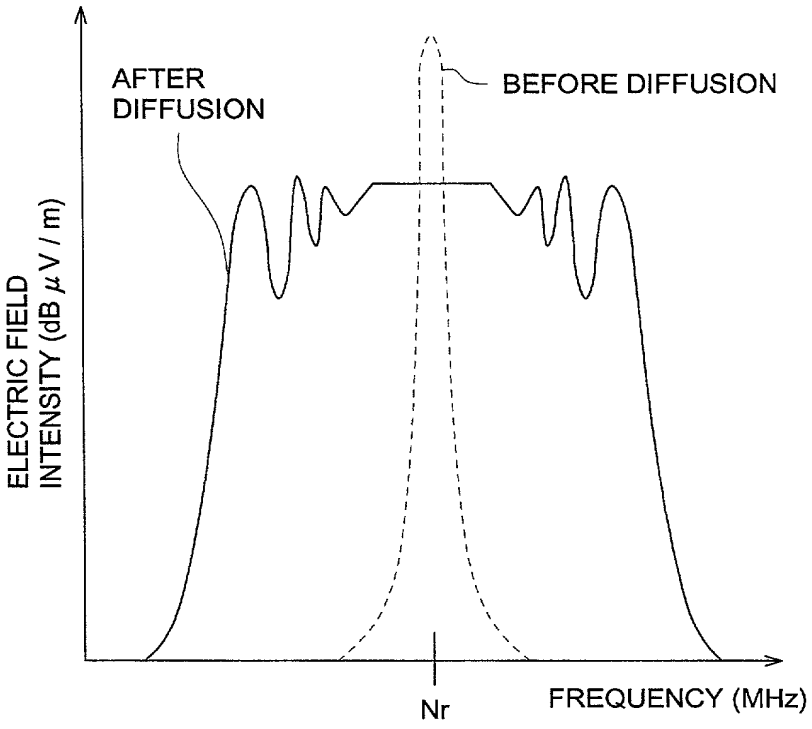

AFTER
DIFFUSION
BEFORE DIFFUSION
ELECTRIC FIELD
INTENSITY (dB μV / m)
Nr
FREQUENCY (MHz)

FIG. 13

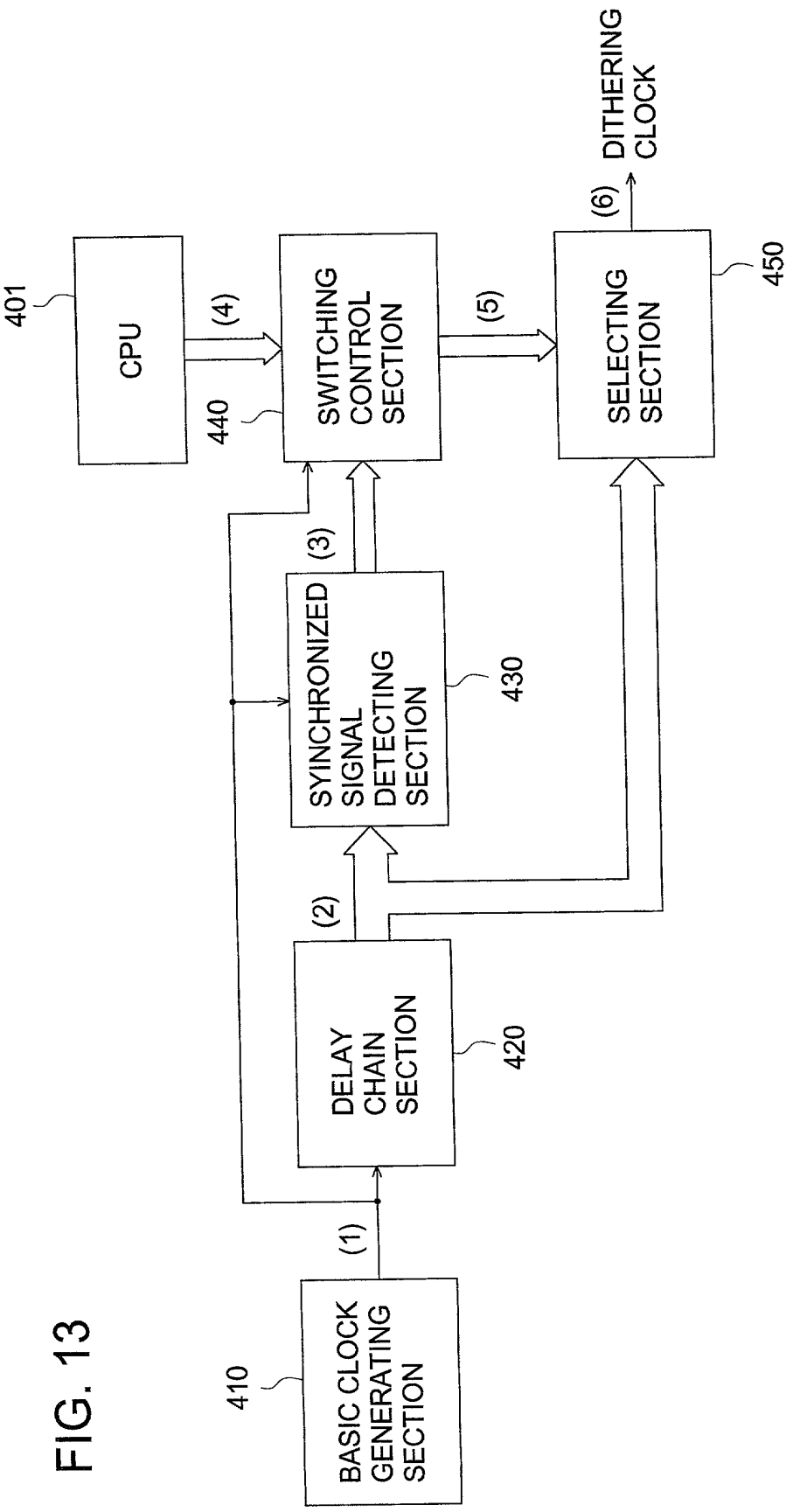

401
CPU
(4)
440
SWITCHING CONTROL SECTION
(5)
SELECTING SECTION
450
(6)
DITHERING CLOCK
(3)
SYINCHRONIZED SIGNAL DETECTING SECTION
430
(2)
DELAY CHAIN SECTION
420
(1)
410
BASIC CLOCK GENERATING SECTION

FIG. 14

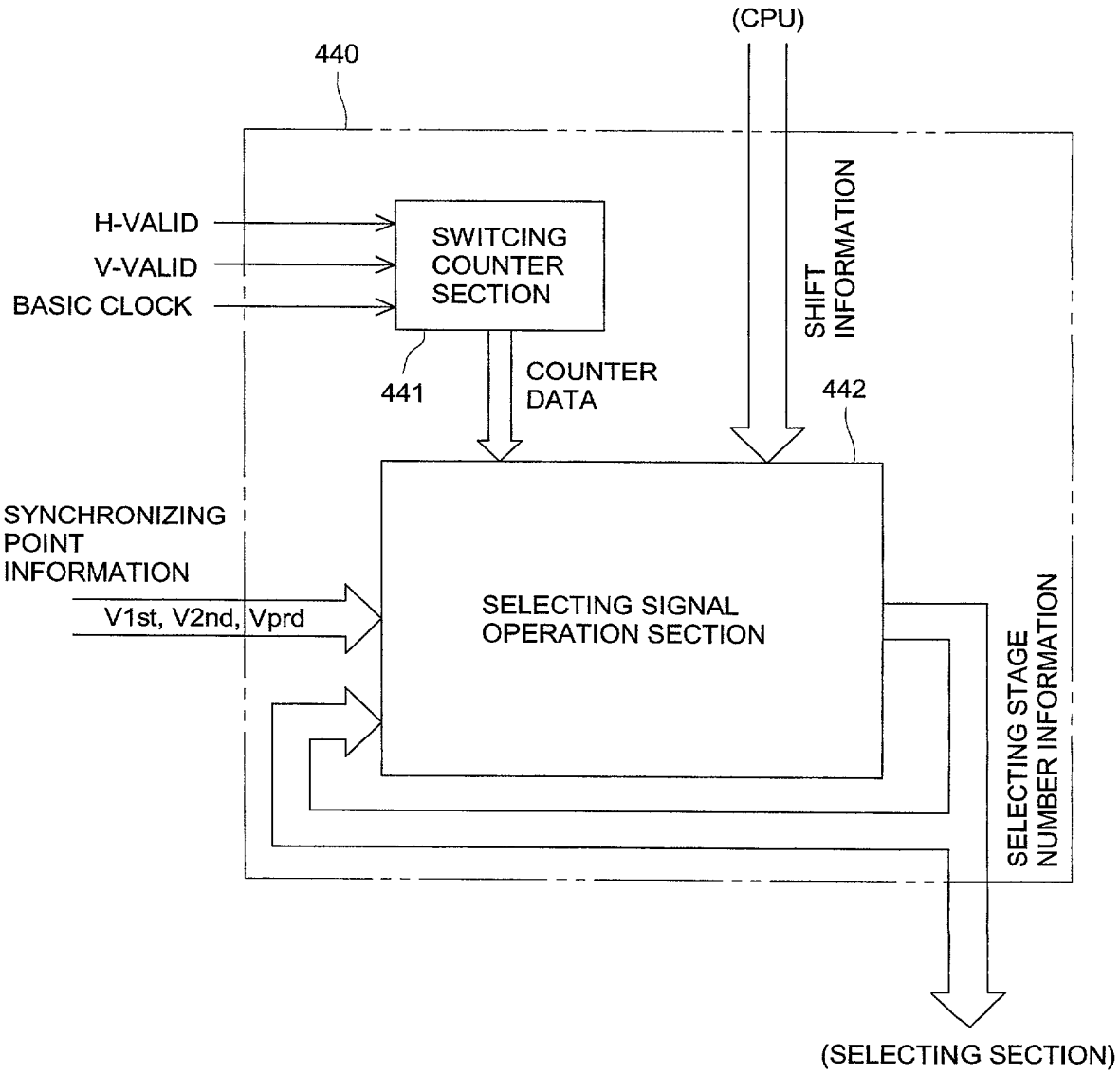

(CPU)
440
H-VALID
V-VALID
BASIC CLOCK
SWITCING COUNTER SECTION
SHIFT INFORMATION
441
COUNTER DATA
442
SYNCHRONIZING POINT INFORMATION
V1st, V2nd, Vprd
SELECTING SIGNAL OPERATION SECTION
SELECTING STAGE NUMBER INFORMATION
(SELECTING SECTION)

FIG. 15

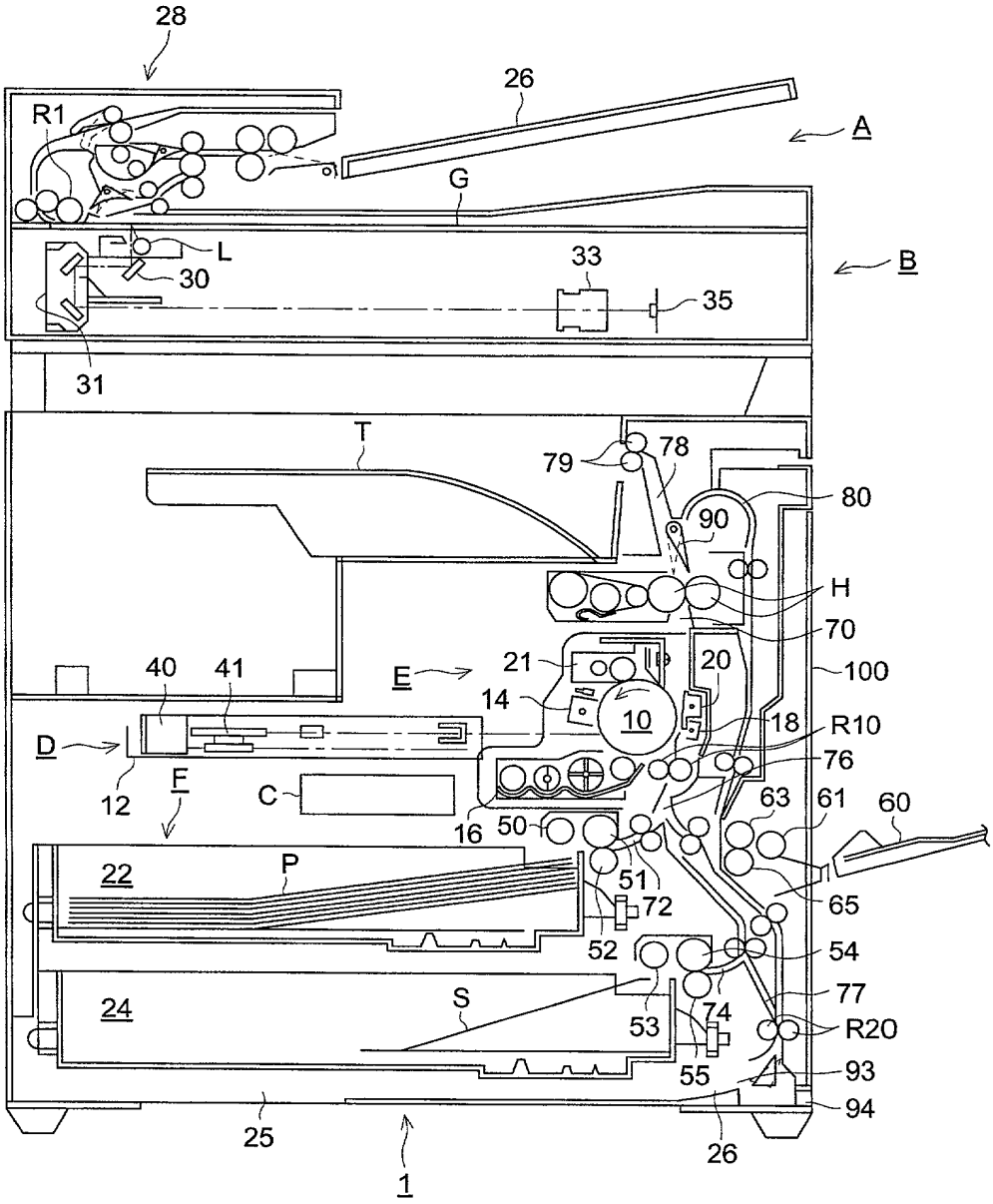

28
26
R1
A
G
L
30
33
35
B
31
T
79
78
80
90
H
70
40
41
E
21
20
100
14
10
18
R10
D
12
F
C
76
16
50
63
61
60
22
P
51
72
65
52
54
24
S
53
74
77
R20
55
93
94
25
26
1

FIG. 16

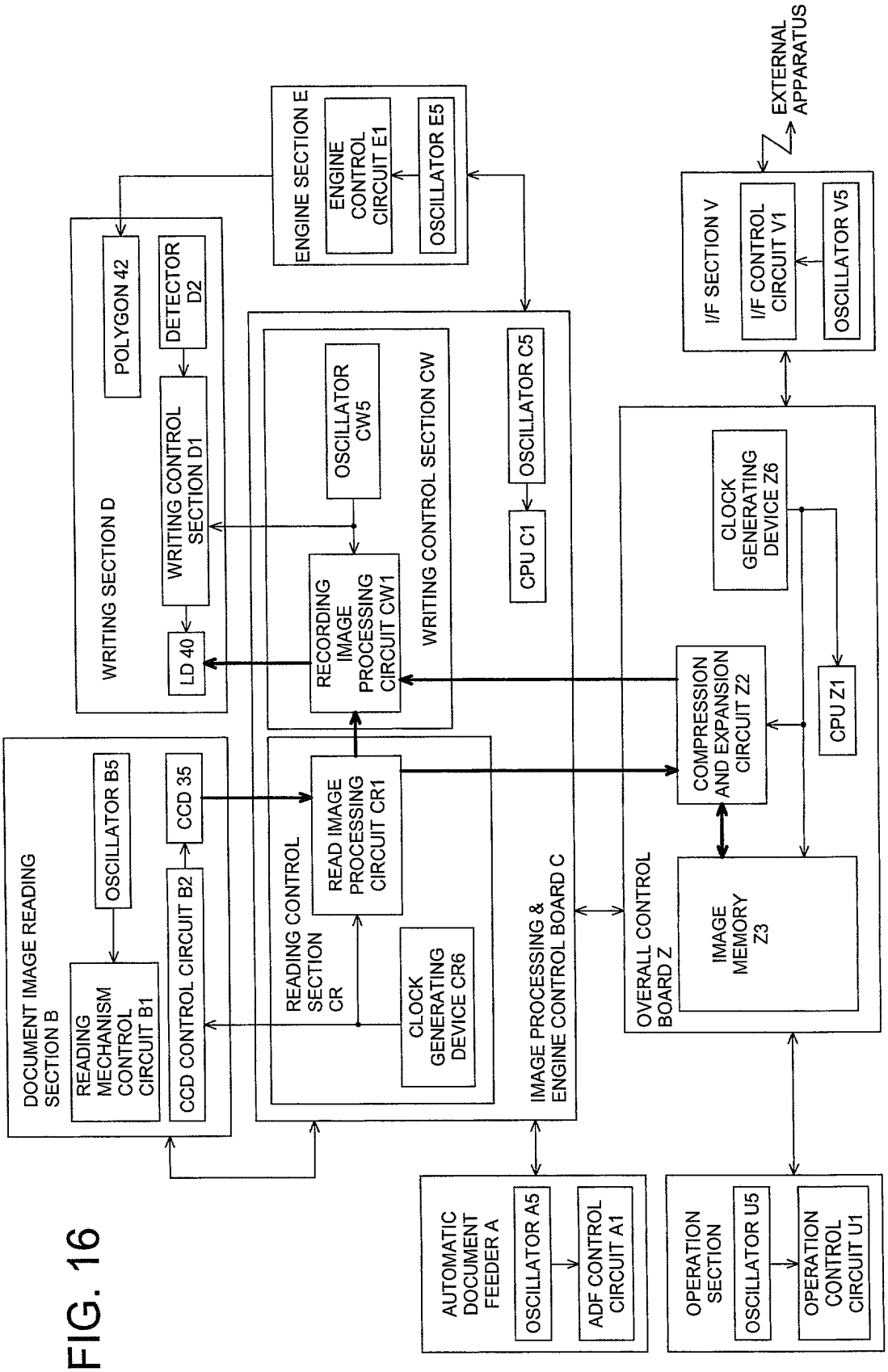

DOCUMENT IMAGE READING SECTION B
READING MECHANISM CONTROL CIRCUIT B1
OSCILLATOR B5
CCD CONTROL CIRCUIT B2
CCD 35
WRITING SECTION D
POLYGON 42
DETECTOR D2
WRITING CONTROL SECTION D1
LD 40
ENGINE SECTION E
ENGINE CONTROL CIRCUIT E1
OSCILLATOR E5
WRITING CONTROL SECTION CW
OSCILLATOR CW5
RECORDING IMAGE PROCESSING CIRCUIT CW1
OSCILLATOR C5
CPU C1
IMAGE PROCESSING & ENGINE CONTROL BOARD C
READING CONTROL SECTION CR
READ IMAGE PROCESSING CIRCUIT CR1
CLOCK GENERATING DEVICE CR6
I/F SECTION V
I/F CONTROL CIRCUIT V1
OSCILLATOR V5
EXTERNAL APPARATUS
OVERALL CONTROL BOARD Z
CLOCK GENERATING DEVICE Z6
COMPRESSION AND EXPANSION CIRCUIT Z2
CPU Z1
IMAGE MEMORY Z3
AUTOMATIC DOCUMENT FEEDER A
OSCILLATOR A5
ADF CONTROL CIRCUIT A1
OPERATION SECTION
OSCILLATOR U5
OPERATION CONTROL CIRCUIT U1

FIG. 17

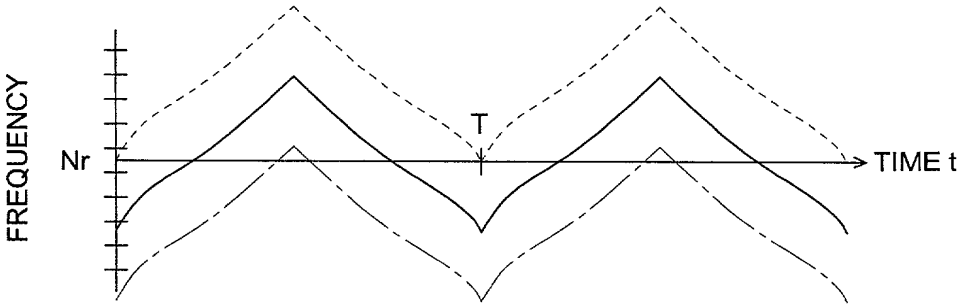


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FIG. 18

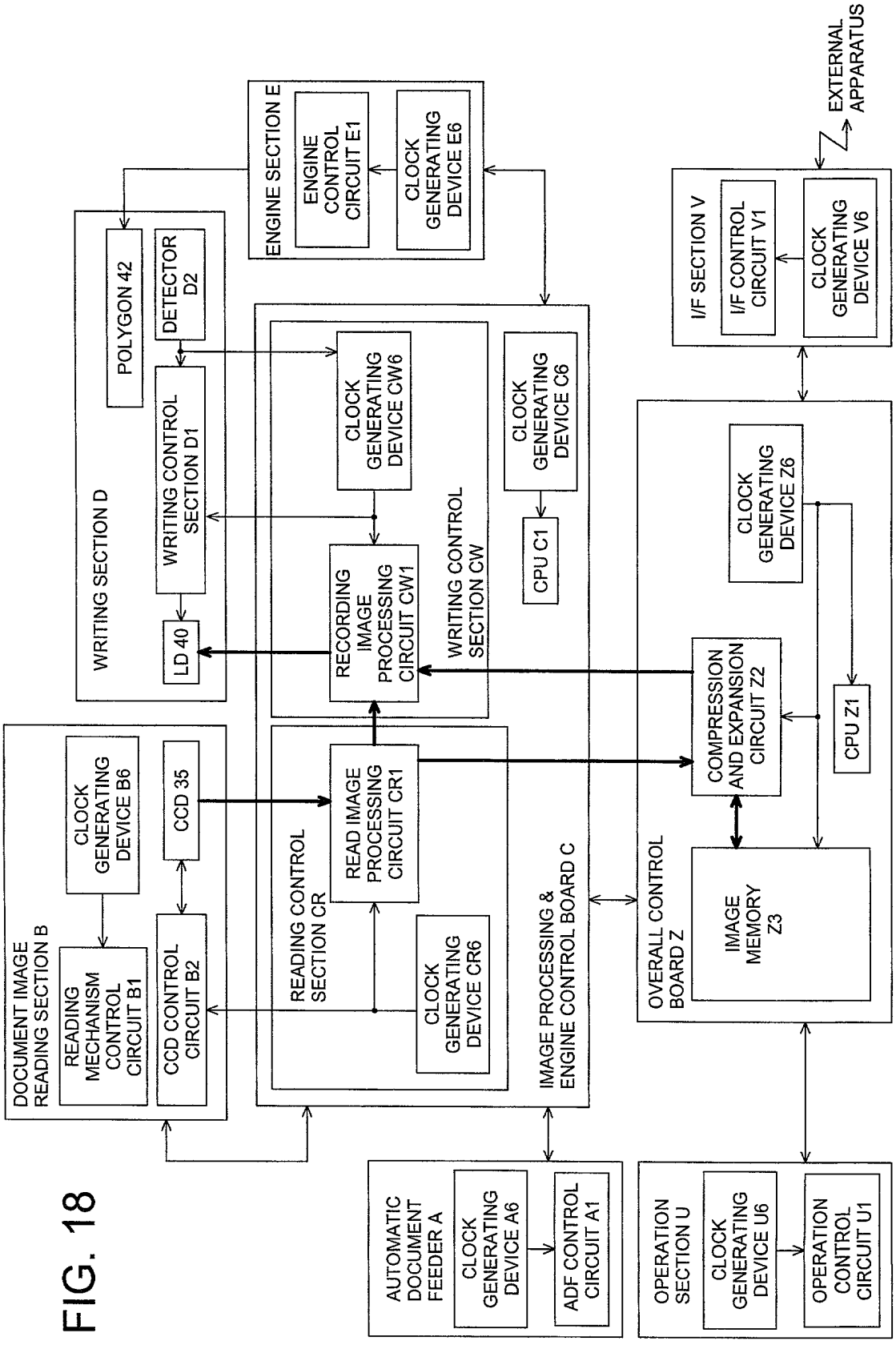
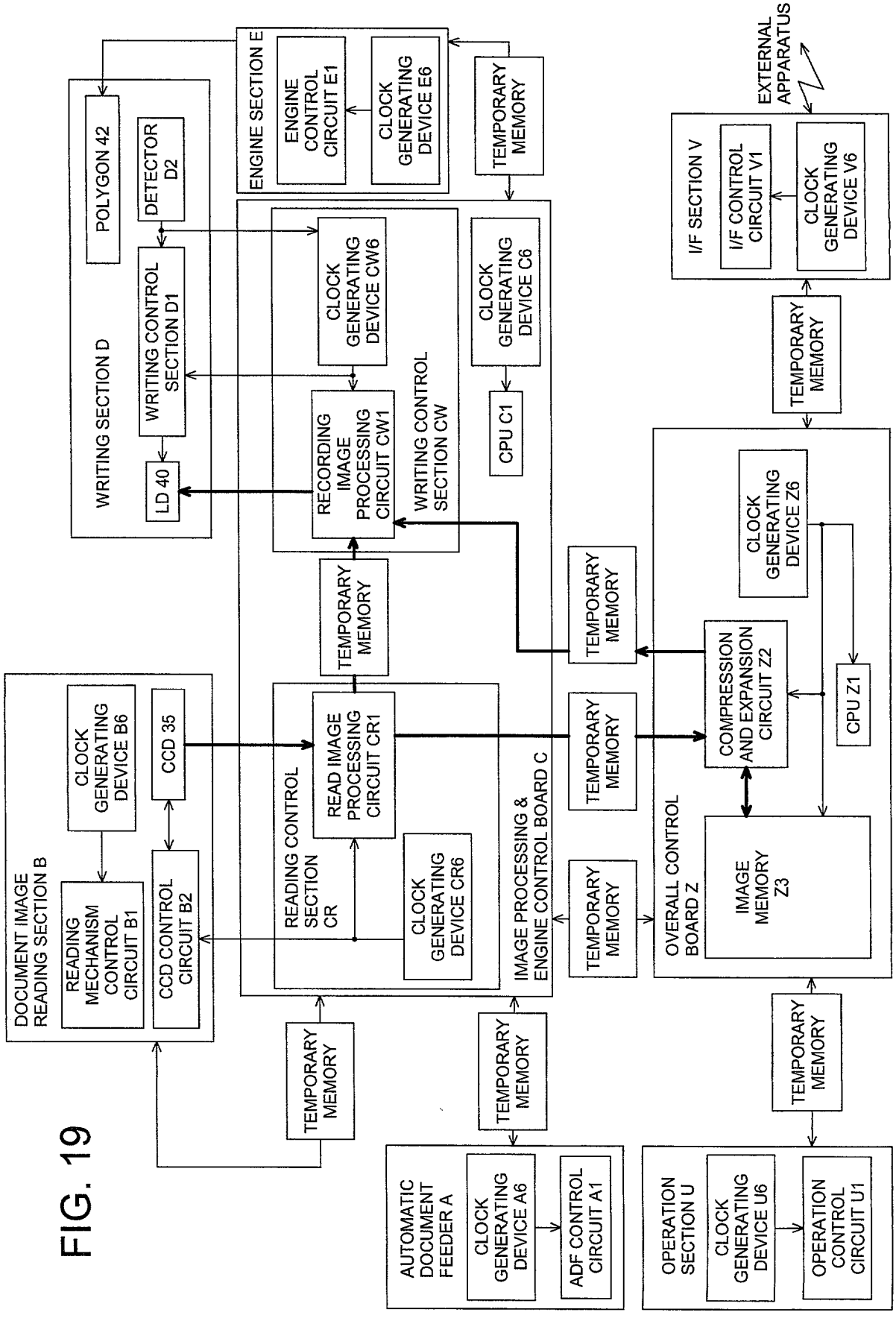

DOCUMENT IMAGE READING SECTION B
READING MECHANISM CONTROL CIRCUIT B1
CLOCK GENERATING DEVICE B6
CCD CONTROL CIRCUIT B2
CCD 35
WRITING SECTION D
POLYGON 42
DETECTOR D2
WRITING CONTROL SECTION D1
LD 40
ENGINE SECTION E
ENGINE CONTROL CIRCUIT E1
CLOCK GENERATING DEVICE E6
IMAGE PROCESSING & ENGINE CONTROL BOARD C
READING CONTROL SECTION CR
READ IMAGE PROCESSING CIRCUIT CR1
CLOCK GENERATING DEVICE CR6
WRITING CONTROL SECTION CW
RECORDING IMAGE PROCESSING CIRCUIT CW1
CLOCK GENERATING DEVICE CW6
CLOCK GENERATING DEVICE C6
CPU C1
OVERALL CONTROL BOARD Z
IMAGE MEMORY Z3
COMPRESSION AND EXPANSION CIRCUIT Z2
CLOCK GENERATING DEVICE Z6
CPU Z1
I/F SECTION V
I/F CONTROL CIRCUIT V1
CLOCK GENERATING DEVICE V6
EXTERNAL APPARATUS
AUTOMATIC DOCUMENT FEEDER A
CLOCK GENERATING DEVICE A6
ADF CONTROL CIRCUIT A1
OPERATION SECTION U
CLOCK GENERATING DEVICE U6
OPERATION CONTROL CIRCUIT U1

FIG. 19


DOCUMENT IMAGE READING SECTION B
READING MECHANISM CONTROL CIRCUIT B1
CLOCK GENERATING DEVICE B6
CCD CONTROL CIRCUIT B2
CCD 35
READING CONTROL SECTION CR
READ IMAGE PROCESSING CIRCUIT CR1
CLOCK GENERATING DEVICE CR6
TEMPORARY MEMORY
IMAGE PROCESSING & ENGINE CONTROL BOARD C
TEMPORARY MEMORY
TEMPORARY MEMORY
TEMPORARY MEMORY
WRITING SECTION D
POLYGON 42
DETECTOR D2
WRITING CONTROL SECTION D1
LD 40
WRITING CONTROL SECTION CW
RECORDING IMAGE PROCESSING CIRCUIT CW1
CLOCK GENERATING DEVICE CW6
CLOCK GENERATING DEVICE C6
CPU C1
ENGINE SECTION E
ENGINE CONTROL CIRCUIT E1
CLOCK GENERATING DEVICE E6
TEMPORARY MEMORY
TEMPORARY MEMORY
OVERALL CONTROL BOARD Z
IMAGE MEMORY Z3
COMPRESSION AND EXPANSION CIRCUIT Z2
CLOCK GENERATING DEVICE Z6
CPU Z1
TEMPORARY MEMORY
I/F SECTION V
I/F CONTROL CIRCUIT V1
CLOCK GENERATING DEVICE V6
EXTERNAL APPARATUS
AUTOMATIC DOCUMENT FEEDER A
CLOCK GENERATING DEVICE A6
ADF CONTROL CIRCUIT A1
TEMPORARY MEMORY
OPERATION SECTION U
CLOCK GENERATING DEVICE U6
OPERATION CONTROL CIRCUIT U1
TEMPORARY MEMORY